IN THE CLAIMS:

Please find below a listing of all of the pending claims. The statuses of the claims are set forth in parentheses.

1. (Currently Amended) A method for minimizing power consumption by a circuit, the method comprising steps of:

determining whether a predetermined period of time has expired, said predetermined period of time being associated with a predetermined period of time to detect a transition of an input or an output of a pipelined circuit having a plurality of stages powered on; and

performing a sequential shut-down procedure on each stage of said plurality of stages of said pipelined circuit in response to said predetermined period of time expiring such that each stage of the plurality of stages is shut-down .

2. (Original) The method of claim 1, further comprising a step of detecting a transition at an input of said pipelined circuit.

3. (Original) The method of claim 2, further comprising a step of performing a turn-on procedure on said pipelined circuit in response to detecting said transition at said input.

4. (Canceled)

5. (Currently Amended) The method of claim 14, wherein said shut-down procedure is performed over multiple clock cycles, and said step of sequentially suppressing power further comprises suppressing power to one of said plurality of stage circuits after each of said multiple clock cycles.

6. (Original) The method of claim 5, wherein said turn-on procedure further comprises a step of sequentially providing power to each of said stage circuits starting from said first stage circuit.

7. (Original) The method of claim 6, wherein said turn-on procedure is performed over multiple clock cycles, and said step of sequentially providing power further comprises providing power to one of said plurality of stage circuits after each of said multiple clock cycles.

8. (Currently Amended) A circuit operable to minimize power consumption by a pipelined circuit, said circuit comprising:

a first transition detection circuit detecting transition of a first signal input to said pipelined circuit;

a second transition detection circuit detecting transition of a second signal output by said pipelined circuit; and

a stage control circuit connected to said first and said second transition detection circuits,~~;~~ said stage control circuit including a timer measuring a predetermined period of time and configured to sequentially control~~ling~~ said power consumption of said pipelined circuit based on a comparison between a signal received from either said first transition detection circuit or said second transition detection circuit and the timer.

9. (Canceled)

10. (Currently Amended) The circuit of claim ~~8~~9, wherein said stage control circuit is operable to suppress power to said pipelined circuit over multiple clock cycles, and power is suppressed to one of said plurality of stage circuits after each of said multiple clock cycles.

11. (Currently Amended) The circuit of claim ~~89~~, wherein said stage control circuit is operable to reset said timer in response to receiving a signal from either said first transition detection circuit or said second transition detection circuit.

12. (Original) The circuit of claim 11, wherein said stage control circuit is operable to provide power to said pipelined circuit in response to resetting said timer.

13. (Original) The circuit of claim 12, wherein said stage control circuit is operable to sequentially provide power to one or more of said plurality of stage circuits starting from said first stage circuit.

14. (Original) The circuit of claim 13, wherein said stage control circuit is operable to provide power to said pipelined circuit over multiple clock cycles, and power is provided to one of said plurality of stage circuits after each of said multiple clock cycles.

15. (Original) The circuit of claim 14, further comprising a buffer circuit connected to an input of said pipelined circuit, said buffer being operable to store data for at least one clock cycle.

16. (Original) A circuit connected to a pipelined circuit and operable to control power provided to said pipelined circuit, said circuit comprising:

an up/down sequencer operable to perform a shut-down procedure or a turn-on procedure to control power applied to a plurality of stage circuits in said pipelined circuit; and

at least one transition detection circuit detecting activity on a bus connected to said pipelined circuit, and said up/down sequencer performing said turn-on procedure in response to said at least one transition detection circuit detecting activity on said bus; and

a timer, wherein said up/down sequencer performing said shut-down procedure in response to said timer expiring.

17. (Original) The circuit of claim 16, wherein said circuit further comprises a multiplexer connected to said timer, said at least one transition detection circuit and said up/down sequencer, whereby said multiplexer transmits a turn-on signal to said up/down sequencer in response to said at least one transition detection circuit detecting activity on said bus, and said multiplexer transmits a shut- down signal to said up/down sequencer in response to said timer expiring.

18. (Original) The circuit of claim 17, wherein said shut-down procedure sequentially suppresses power supplied to said plurality of stage circuits.

19. (Original) The circuit of claim 18, wherein said turn-on procedure sequentially supplies power to said plurality of stage circuits.

20. (Original) The circuit of claim 19, wherein said at least one transition detection circuit comprises one or more of a front-end transition detection circuit operable to detect activity on a bus connected to a front-end of said pipelined circuit and aback-end transition detection circuit operable to detect activity on a bus connected to an output of said pipelined circuit.

21. (New) A system for minimizing power consumption by a pipelined circuit having a plurality of stages, said system comprising:

means for detecting an amount of time since said pipelined circuit sent an output signal;

means for comparing said amount of time to a predetermined amount of time; and

means for sequentially reducing power to each stage of said plurality of stages if said amount of time is greater than said predetermined amount of time.

22. (New) The system of claim 21, further comprising:

means for detecting a second amount of time since said pipelined circuit received an input signal;

means for comparing said second amount of time to a second predetermined amount of time; and

means for sequentially increasing power to each stage of said plurality of stages if said second amount of time is greater than said second predetermined amount of time.

23. (New) The system of claim 22, further comprising:

means for arbitrating between said means for detecting said first amount of time and said means for detecting said second amount of time to determine whether to activate said means for sequentially increasing power or said means for sequentially decreasing power.